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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Wendell P. Noble et al.

Title: CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR

Attorney Docket No.: 303.379US2

PATENT APPLICATION TRANSMITTAL

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items and information (as indicated with an "X"):

X **DIVISIONAL** of prior Patent Application No. 08/939,742 (under 37 CFR § 1.53(b)) comprising:
- X Specification (22 pgs, including claims numbered 1 through 26 and a 1 page Abstract).
- X Formal Drawing(s) (16 sheets).
- X Copy of signed Combined Declaration and Power of Attorney (6 pgs) from prior application.
- X Incorporation by Reference: *The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied herewith, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.*
- X Check in the amount of $690.00 to pay the filing fee.

X Prior application is assigned of record to Micron Technology, Inc..

X Information Disclosure Statement (1 pgs), Form 1449 (13 pgs). References NOT enclosed, cited in prior application.

X Preliminary Amendment (1 pgs).

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The filing fee has been calculated below as follows:

	No. Filed	No. Extra	Rate	Fee
TOTAL CLAIMS	7 - 20 =	0	x 18 =	$0.00
INDEPENDENT CLAIMS	2 - 3 =	0	x 78 =	$0.00
[ ] MULTIPLE DEPENDENT CLAIMS PRESENTED				$0.00
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Wendell P. Noble et al.	Examiner: Unknown
Serial No.:	Unknown	Group Art Unit: Unknown
Filed:	Herewith	Docket: 303.379US2
Title:	CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR	

PRELIMINARY AMENDMENT

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

Before taking up the above identified application for examination, please amend it as follows:

IN THE SPECIFICATION

At the first line after the title, insert thereto: "This application is a Divisional of U.S. Application No. 08/939,742, filed October 6, 1997."

IN THE CLAIMS

Please cancel claims 1-19. Claims 20-26 therefore remain pending in the application.

Applicant will file additional claims in a Supplemental Preliminary Amendment. The Examiner is invited to contact Applicants' representatives at the below-listed telephone number if examination begins before receiving the additional claims.

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Respectfully submitted,

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Circuit and Method for a Folded Bit Line Memory Cell With Vertical Transistor and Trench Capacitor

Technical Field of the Invention

The present invention relates generally to the field of memory devices and, in particular, to a circuit and method for a folded bit line memory cell with a vertical transistor and a trench capacitor.

Background of the Invention

Electronic systems typically store data during operation in a memory device. In recent years, the dynamic random access memory (DRAM) has become a popular data storage device for such systems. Basically, a DRAM is an integrated circuit that stores data in binary form (e.g., "1" or "0") in a large number of cells. The data is stored in a cell as a charge on a capacitor located within the cell. Typically, a high logic level is approximately equal to the power supply voltage and a low logic level is approximately equal to ground.

The cells of a conventional DRAM are arranged in an array so that individual cells can be addressed and accessed. The array can be thought of as rows and columns of cells. Each row includes a word line that interconnects cells on the row with a common control signal. Similarly, each column includes a bit line that is coupled to at most one cell in each row. Thus, the word and bit lines can be controlled so as to individually access each cell of the array.

A memory array is typically implemented as an integrated circuit on a semiconductor substrate in one of a number of conventional layouts. One such layout is referred to as an "folded digit line" architecture. In this architecture, sense amplifier circuits are provided at the edge of the array. The bit lines are paired in complementary pairs. Each complementary pair in the array feeds into a sense amplifier circuit. The sense amplifier circuit detects and amplifies differences in voltage on the complementary pair of bit lines as described in more detail below.

To read data out of a cell, the capacitor of a cell is accessed by selecting the word line associated with the cell. A complementary bit line that is paired with the bit line for the selected cell is equilibrated with the voltage on the bit line for the selected cell. The equilibration voltage is typically midway between the high and low logic levels. Thus, conventionally, the bit lines are equilibrated to one-half of the power supply voltage, $V_{CC}/2$. When the word line is activated for the selected cell, the capacitor of the selected cell discharges the stored voltage onto the bit line, thus changing the voltage on the bit line.

The sense amplifier detects and amplifies the difference in voltage on the pair of bit lines. The sense amplifier typically includes two main components: an n-sense amplifier and a p-sense amplifier. The n-sense amplifier includes a cross-coupled pair of n-channel transistors that drive the low bit line to ground. The p-sense amplifier includes a cross-coupled pair of p-channel transistors and is used to drive the high bit line to the power supply voltage.

An input/output device for the array, typically an n-channel transistor, passes the voltage on the bit line for the selected cell to an input/output line for communication to, for example, a processor of a computer or other electronic system associated with the DRAM. In a write operation, data is passed from the input/output lines to the bit lines by the input/output device of the array for storage on the capacitor in the selected cell.

Each of the components of a memory device are conventionally formed as part of an integrated circuit on a "chip" or wafer of semiconductor material. One of the limiting factors in increasing the capacity of a memory device is the amount of surface area of chip used to form each memory cell. In the industry terminology, the surface area required for a memory cell is characterized in terms of the minimum feature size, "F," that is obtainable by the lithography technology used to form the memory cell. Conventionally, the memory cell is laid out with a transistor that includes first and second source/drain regions separated by a body or gate region that are disposed horizontally along a surface of the chip. When isolation between adjacent transistors is considered, the surface area required for such a transistor is generally $8F^2$ or $6F^2$.

Some researchers have proposed using a vertical transistor in the memory cell in order to reduce the surface area of the chip required for the cell. Each of these proposed memory cells, although smaller in size from conventional cells, fails to provide adequate operational characteristics when compared to more conventional structures. For example, U.S. Patent No. 4,673,962 (the '962 Patent) issued to Texas Instruments on June 16, 1997. The '962 Patent discloses the use of a thin poly-silicon field effect transistor (FET) in a memory cell. The poly-silicon FET is formed along a sidewall of a trench which runs vertically into a substrate. At a minimum, the poly-silicon FET includes a junction between poly-silicon channel 58 and the bit line 20 as shown in Figure 3 of the '962 Patent. Unfortunately, this junction is prone to charge leakage and thus the poly-silicon FET may have inadequate operational qualities to control the charge on the storage capacitor. Other known disadvantages of such thin film poly-silicon devices may also hamper the operation of the proposed cell.

Other researchers have proposed use of a "surrounding gate transistor" in which a gate or word line completely surrounds a vertical transistor. *See, e.g., Impact of a Vertical Φ-shape transistor (VΦT) Cell for 1 Gbit DRAM and Beyond*, IEEE Trans. On Elec. Devices, Vol 42, No.12, December, 1995, pp. 2117-2123. Unfortunately, these devices suffer from problems with access speed due to high gate capacitance caused by the increased surface area of the gate which slows down the rise time of the word lines. Other vertical transistor cells include a contact between the pass transistor and a poly-silicon plate in the trench. Such vertical transistor cells are difficult to implement due to the contact and should produce a low yield.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for realizable memory cell that uses less surface area than conventional memory cells.

Summary of the Invention

The above mentioned problems with memory cells and other problems are addressed by the present invention and which will be understood by reading and studying the following specification. A memory cell is described which includes a vertical transistor and trench capacitor.

In particular, an illustrative embodiment of the present invention includes a memory cell for a memory array with a folded bit line configuration. The memory cell includes an access transistor that is formed in a pillar of single crystal semiconductor material. The access transistor has first and second sources/drain regions and a body region that are vertically aligned. The access transistor also includes a gate that is coupled to a wordline disposed adjacent to the body region of the access transistor. A passing wordline is separated from the gate by an insulator for coupling to other memory cells adjacent to the memory cell. A trench capacitor is also included. The trench capacitor includes a first plate that is formed integral with the first source/drain region of the access transistor and a second plate that is disposed adjacent to the first plate and separated from the first plate by a gate oxide. In another embodiment, the second plate of the trench capacitor surrounds the second source/drain region. In another embodiment, an ohmic contact is included to couple the second plate to a layer of semiconductor material.

In another embodiment, a memory device is provided. The memory device includes an array of memory cells. Each memory cell includes a vertical access transistor that is formed of a single crystalline semiconductor pillar that extends outwardly from a substrate. The semiconductor pillar includes a body and first and second source/drain regions. A gate is disposed adjacent to a side of the pillar adjacent to the body region. The memory cell also includes a trench capacitor wherein a first plate of the trench capacitor is integral with the first source/drain region and a second plate of the trench capacitor is disposed adjacent to the first plate. The memory device also includes a number of bit lines that are each selectively coupled to a number of the memory cells at the second source/drain region of the access transistor. This forms

columns of memory cells in a folded bit line configuration. Finally, the memory device also includes a number of wordlines. The wordlines are disposed substantially orthogonal to the bit lines in trenches between rows of the memory cells. Each trench includes two wordlines. Each wordline is coupled to gates of alternate access transistors on opposite sides of the trench. In another embodiment, the pillars extend outward from a semiconductor portion of the substrate. In another embodiment, a surface area of the memory cell is four F^2, wherein F is a minimum feature size. In another embodiment, a second plate of the trench capacitor surrounds the second source/drain region of the access transistor. In another embodiment, the second plate of the trench capacitor is maintained at approximately ground potential. In another embodiment, the pillar has a sub-micron width so as to allow substantially full depletion of the body region.

In another embodiment, a memory array is provided. The memory array includes a number of memory cells forming an array with a number of rows and columns. Each memory cell includes an access transistor with body and first and second source/drain regions formed vertically, outwardly from a substrate. A gate is disposed adjacent to a side of the transistor. The memory array includes a number of first isolation trenches that separate adjacent rows of memory cells. First and second wordlines are disposed in each of the first isolation trenches. The first and second wordlines are coupled to alternate gates on opposite sides of the trench. The memory array also includes a number of second isolation trenches, each substantially orthogonal to the first isolation trenches and intraposed between the adjacent memory cell.

In another embodiment, a method of fabricating a memory array is provided. A number of access transistors were formed wherein each access transistor is formed in a pillar of semiconductor material that extends outwardly from a substrate. The access transistor includes a first source/drain region, a body region and second source/drain region that are formed vertically. The method also includes forming a trench capacitor wherein a first plate of the trench capacitor is integral with the first source/drain region of the access transistor. Further, the method includes forming a number of wordlines in a number of trenches that separates adjacent rows of access transistors. Each trench

includes two wordlines with the gate of each wordline interconnecting alternate access transistors on opposite sides of the trench. Finally, the method includes a number of bit lines that interconnect second source/drain regions of selected access transistors.

In another embodiment, a method of fabricating a memory is provided. The method begins with forming a first conductivity type first source/drain region layer on a substrate. A second conductivity type body region layer is formed on the first source/drain region layer. A first conductivity type second source/drain region layer is formed on the body region layer. Additionally, a plurality of substantially parallel column isolation trenches are formed extending through the second source/drain region layer, the body region layer and the first source/drain region layer. This provides column bars between the column isolation trenches. Further, a plurality of substantially parallel row isolation trenches are formed orthogonal to the column isolation trenches and extending to substantially the same depth as the column isolation trenches. This produces an array of vertical access transistors for the memory array. The row and column isolation trenches are filled with a conductive material to a level that does not exceed the lower level of the body region so as to provide a common plate for capacitors of the memory cells of the memory array. Two conductive wordlines are formed in each row isolation trench to selectively interconnect alternate access transistors on opposite sides of the row isolation trench. Finally, bit lines are formed to selectively interconnect the second source/drain regions of the access transistors on each column.

Brief Description of the Drawings

Figure 1 is a block/schematic diagram of an illustrative embodiment of the present invention that includes a memory device that is coupled to an electronic system;

Figure 2 is a plan view of an illustrative embodiment of a layout for a memory array according to the teachings of the present invention;

Figure 3 is a perspective view of the illustrative embodiment of figure 2;

Figure 4 is a schematic diagram of a memory cell of the embodiment of Figures 2 and 3; and

Figures 5A through 5M are perspective and elevational views of an embodiment of an integrated circuit that illustrate processing steps for fabricating the integrated circuit according to the teachings of the present invention.

Detailed Description of the Invention

In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. The embodiments are intended to describe aspects of the invention in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and logical, mechanical and electrical changes may be made without departing from the scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense.

In the following description, the terms wafer and substrate are interchangeably used to refer generally to any structure on which integrated circuits are formed, and also to such structures during various stages of integrated circuit fabrication. Both terms include doped and undoped semiconductors, epitaxial layers of a semiconductor on a supporting semiconductor or insulating material, combinations of such layers, as well as other such structures that are known in the art.

The term "horizontal" as used in this application is defined as a plane parallel to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate. The term "vertical" refers to a direction perpendicular to the horizonal as defined above. Prepositions, such as "on", "side" (as in "sidewall"), "higher", "lower", "over" and "under" are defined with respect to the conventional plane or surface being on the top surface of the wafer or substrate, regardless of the orientation of the wafer or substrate.

Figure 1 is a block/schematic diagram that illustrates generally one embodiment of a memory device 100 incorporating an array of memory cells constructed according to the teachings of the present invention. Memory device 100 is coupled to electronic system 101. Electronic system 101 may comprise, for example, a microprocessor, a memory controller, a chip set or other appropriate electronic system. Memory device 100 illustrates, by way of example but not by way of limitation, a dynamic random access memory (DRAM), in a folded bit line configuration. Memory device 100 includes array 110 with N word lines and M complementary bit line pairs. Array 110 further includes memory cells 112-*ij*, where *i* refers to the word line of the cell and *j* refers to the bit line of the cell. It is noted that an asterisk (*) is used to indicate a cell that is associated with a complementary bit line.

In the exemplary embodiment of Figure 1, each of memory cells 112-*ij* has a substantially identical structure, and accordingly, only one memory cell is described herein. These memory cells 112-*ij* include a vertical transistor where one plate of a capacitor is integral with the transistor.

The vertical transistors are laid out in a substantially checker-board pattern of rows and columns on a substrate. Memory cell 112-11 includes vertical transistor 130-11. A source/drain region of transistor 130-11 is formed in a deep trench and extends to a sufficient depth to form a storage node of storage capacitor 132-11. The other terminal of storage capacitor 132-11 is part of a mesh or grid of poly-silicon that surrounds the source/drain region of transistor 130-11 and is coupled to ground potential.

The N word lines, WL-1 through WL-N, are formed in trenches that separate adjacent rows of vertical transistors 130-*ij*. Each trench houses two word lines, with each word line in a trench acting as a gate for alternate transistors on one side of the trench.

Bit lines BL-1 through BL-M are used to write to and read data from memory cells 112-*ij* in response to addressing circuitry. For example, address buffer 114 is coupled to control bit line decoder 118, which also includes sense amplifiers and

input/output circuitry that is coupled to bit lines BL-1 through BL-M and complement bit lines BL-1* through BL-M*of array 110. Address buffer 114 also is coupled to control word line decoder 116. Word line decoder 116 and bit line decoder 118 selectably access memory cells 112-*ij* in response to address signals that are provided on address lines 120 from electronic system 101 during write and read operations.

In operation, memory 100 receives an address of a particular memory cell at address buffer 114. For example, electronic system 101 may provide address buffer 114 with the address for cell 112-11 of array 110. Address buffer 114 identifies word line WL-1 for memory cell 112-11 to word line decoder 116. Word line decoder 116 selectively activates word line WL-1 to activate access transistor 130-1*j* of each memory cell 112-1*j* that is connected to word line WL-1. Bit line decoder 118 selects bit line BL-1 for memory cell 112-11. For a write operation, data received by input/output circuitry is coupled to bit lines BL-1 through access transistor 130-11 to charge or discharge storage capacitor 132-11 of memory cell 112-11 to represent binary data. For a read operation, bit line BL-1 of array 110 is equilibrated with bit line BL-1*. Data stored in memory cell 112-11, as represented by the charge on its storage capacitor 132-11, is coupled to bit line BL-1 of array 110. The difference in charge in bit line BL-1 and bit line BL-1* is amplified, and a corresponding voltage level is provided to the input/output circuits.

Figures 2 through 4 illustrate an embodiment of a memory cell with a vertical transistor and trench capacitor for use, for example, in memory device 100 of Figure 1. Specifically, Figure 2 is a plan view of a layout of a number of memory cells indicated generally at 202A through 202D in array 200. Figure 2 depicts only four memory cells. It is understood, however, that array 200 may include a larger number of memory cells even though only four are depicted here.

Each memory cell is constructed in a similar manner. Thus, only memory cell 202C is described herein in detail. Memory cell 202C includes pillar 204 of single crystal semiconductor material, e.g., silicon, that is divided into first source/drain region 206, body region 208, and second source/drain region 210 to form access transistor 211.

Pillar 204 extends vertically outward from substrate 212 of, for example, p- silicon. First source/drain region 206 and second source/drain region 210 each comprise, for example, n + silicon and body region 208 comprises p- silicon.

Word line 212 passes body region 208 of access transistor 211 in isolation trench 214. Word line 212 is separated from body region 208 of access transistor 211 by gate oxide 216 such that the portion of word line 212 adjacent to body region 208 operates as a gate for access transistor 211. Word line 212 may comprise, for example, n+ poly-silicon material that is deposited in isolation trench 214 using an edge-defined technique such that word line 212 is less than a minimum feature size, F, for the lithographic technique used to fabricate array 200. Passing word line 213 is also formed in trench 214. Cell 202C is coupled with cell 202B by bit line 218.

Memory cell 202C also includes storage capacitor 219 for storing data in the cell. A first plate of capacitor 219 for memory cell 202C is integral with second source/drain region 210 of access transistor 211. Thus, memory cell 202C may be more easily realizable when compared to conventional vertical transistors since there is no need for a contact between second source/drain region 210 and capacitor 219. Second plate 220 of capacitor 219 is common to all of the capacitors of array 200. Second plate 220 comprises a mesh or grid of n+ poly-silicon formed in deep trenches that surrounds at least a portion of second source/drain region 210 of each pillar 204A through 204D. Second plate 220 is grounded by contact with substrate 212 underneath the trenches. Second plate 220 is separated from source/drain region 210 by gate oxide 222.

With this construction for memory cell 202C, access transistor 211 is like a silicon on insulator device. Three sides of the transistor are insulated by thick oxide in the shallow trench. If the doping in pillar 204 is low and the width of the post is sub-micron, then body region 208 can act as a "fully-depleted" silicon on insulator transistor with no body or substrate to contact. This is desirable to avoid floating body effects in silicon on insulated transistors and is achievable due to the use of sub-micron dimensions in access transistor 211.

Figure 4 is a schematic diagram that illustrates an effective circuit diagram for the embodiment of Figures 2 and 3. It is noted that storage capacitor 219 formed by second source/drain region 210 and second plate 220 is depicted as four separate capacitors. This represents that the second plate 220 surrounds second source/drain region 210 which increases the charge storage capacitance and stored charge for the memory cell. It is also noted that second plate 220 is maintained at a constant potential, e.g., ground potential.

As shown in Figure 2, the memory cells of array 200 are four-square feature ($4F^2$) memory cells. Using cell 202D as an example, the surface area of cell 202D is calculated based on linear dimensions in the bit line and word line directions. In the bit line direction, the distance from one edge of cell 202D to a common edge of adjacent cell 202A is approximately 2 minimum feature sizes (2F). In the word line direction, the dimension is taken from the midpoint of isolation trenches on either side of memory cell 202D. Again, this is approximately two minimum feature sizes (2F). Thus, the size of the cell is $4F^2$. This size is much smaller than the current cells with stacked capacitors or trenched capacitors.

Figures 5A through 5M illustrate one embodiment of a process for fabricating an array of memory cells, indicated generally at 299, according to the teachings of the present invention. In this example, dimensions are given that are appropriate to a 0.2 micrometer lithographic image size. For other image sizes, the vertical dimensions can be scaled accordingly.

As shown in Figure 5A, the method begins with substrate 300. Substrate 300 comprises, for example, a P-type silicon wafer, layer of P- silicon material, or other appropriate substrate material. Layer 302 is formed, for example, by epitaxial growth outwardly from layer 300. Layer 302 comprises single crystalline N+ silicon that is approximately 3.5 micrometers thick. Layer 304 is formed outwardly from layer 302 by epitaxial growth of single crystalline P- silicon of approximately 0.5 microns. Layer 306 is formed by ion implantation of donor dopant into layer 304 such that layer 306 comprises single crystalline N+ silicon with a depth of approximately 0.1 microns.

A thin layer of silicon dioxide (SiO_2), referred to as pad oxide 308, is deposited or grown on layer 306. Pad oxide 308 has a thickness of approximately 10 nanometers. A layer of silicon nitride (Si_3N_4), referred to as pad nitride 310, is deposited on pad oxide 308. Pad nitride 310 has a thickness of approximately 200 nanometers.

Photo resist layer 312 is deposited outwardly from layer 310. Photo resist layer 312 is patterned with a mask to define openings 314 in layer 312 to be used in selective etching. As shown in Figure 5B, column isolation trenches 316 are etched through openings 314 in photo resist layer 312 in a direction parallel to which the bit lines will be formed. Column isolation trenches 316 extend down through nitride layer 310, oxide layer 308, N+ layer 306, P- layer 304, N+ layer 302, and into substrate 300.

A thin thermal protective oxide layer 318 is grown on exposed surfaces of substrate 300 and layers 302, 304, and 306. Layer 318 is used to protect substrate 300 and layers 302, 304 and 306 during subsequent process step.

A layer of intrinsic poly-silicon 320 is deposited by chemical vapor deposition (CVD) to fill column isolation trenches 316. Layer 320 is etched by reactive ion etching (RIE) such that layer 320 is recessed below a top of layer 302. Layer 322 of silicon nitride (Si_3N_4) is deposited by, for example, chemical vapor deposition to fill trenches 316. Layer 322 is planarized back to a level of layer 310 using, for example, chemical mechanical polishing (CMP) or other suitable planarization technique to produce the structure shown in Figure 5C.

As shown in Figure 5D, layer 324 of photo resist material is deposited outwardly from nitride layers 322 and 310. Layer 324 is exposed through a mask to define openings 326 in layer 324. Openings 326 are orthogonal to trenches 316 that were filled by intrinsic poly-silicon layer 320 and nitride layer 322. Next, nitride layers 310 and 322 are etched to a depth sufficient to expose a working surface 328 of layer 306. It is noted that at this point layer 320 of intrinsic poly-silicon is still covered by a portion of nitride layer 322.

As shown in Figure 5E, the portion of layers 306, 304, and 302 that are exposed in openings 326 are selectively etched down to a distance approximately equal to

column isolation trenches 316. A thin thermal protective oxide is grown on the exposed silicon of layers 302, 304 and 306 as well as an exposed upper surface of layer 300. This oxide layer is labeled 330 in Figure 5E.

As shown in Figure 5F, the remaining nitride layer 322 exposed in openings 326 is directionally etched to expose layer of intrinsic poly-silicon 320. It is noted that nitride layer 322 and nitride layer 310 remain intact under the photo resist layer 324. Layer of intrinsic poly-silicon 320 is next isotropically etched using a silicon etchant which does not attack oxide or nitride layers. Next, an isotropic oxide etch is performed to remove all exposed thin oxide. The photo resist layer 324 is removed. At this point, the method has produced the structure shown in Figure 5G. This structure includes a nitride bridge formed from nitride layers 310 and 322 that extends orthogonal to column isolation trenches 316 and covers the remaining portions of layers 302, 304, and 306. The structure also includes row isolation trenches 322 that are orthogonal to column isolation trenches 316. The structure of Figure 5G also includes pillars 334A through 334D of single crystal silicon material. Pillars 334A through 334D form the basis for individual memory cells for the memory array formed by the process.

An optional metal contact 336 may be formed by, for example, deposition of a collimated refractory metal deposition, e.g., titanium, tungsten, or a similar refractory metal. This provides an ohmic metal contact for a capacitor plate on a surface 335 of substrate 300.

Dielectric layer 338 is deposited or grown on sidewalls of layer 302 of pillars 334A through 334D. Layer 338 acts as the dielectric for the storage capacitors of array 299 of memory cells. If contact 336 was previously deposited on a surface of substrate 300, dielectric layer 338 should be directionally etched to clear dielectric material from the bottom of row isolation trench 332.

Next, a common plate for all of the memory cells of array 299 is formed by a chemical vapor deposition of N+ poly-silicon or other appropriate refractory conductor in column isolation trenches 316 and row isolation trenches 322. In this manner, conductor mesh or grid 340 is formed so as to surround each of pillars 334A through

334D. Mesh 340 is planarized and etched back to a level approximately at the bottom of the nitride bridge formed by nitride layers 322 and 310 as shown in Figure 5H. An additional etch is performed to remove any remaining exposed capacitor dielectric of layer 338 from the sides of semiconductor pillars 334A through 334D.

Referring to Figure 5I, layer 350 of silicon nitride (Si_3N_4) is formed by, for example, chemical vapor deposition to a thickness of approximately 20 nanometers. Layer 350 is directionally etched to leave silicon nitride on sidewalls 352 of pillars 344B and 344C as shown in Figure 5I. It is noted that silicon nitride is also deposited on the sidewalls of pillars 334A and 334B. Layer 354 of thermal silicon dioxide (SiO_2) is grown or deposited to a depth of approximately 100 nanometers on exposed surfaces 356 of mesh 340. Layer 350 is then removed.

Referring to Figure 5J, layer 358 of intrinsic poly-silicon is deposited, for example, by chemical vapor deposition with a thickness of approximately 50 nanometers. Layer 358 is directionally etched to the leave intrinsic poly-silicon on sidewalls 352 of pillars 334B and 334C as shown in Figure 5J. It is noted that layer 358 is also formed on pillars 334A and 334D.

As shown in Figures 5J and 5K, layer 360 of photo resist material is deposited and masked to expose alternate sidewalls 352 of pillars 334A through 334D. Exposed portions of layer 358 in openings 362 through photo resist layer 360 are selectively etched to expose sidewalls 352 of pillars 334A through 334D. Photo resist layer 360 is removed and gate oxide layer 364 is grown on exposed sidewalls 352 of pillars 334A through 334D. Additionally, gate oxide layer 364 is also deposited on remaining intrinsic poly-silicon layers 358.

Referring to Figure 5L, word line conductors 366 are deposited by, for example, chemical vapor deposition of n + poly-silicon or other refractory metal to a thickness of approximately 50 nanometers. Conductors 366 are directionally and selectively etched to leave on sidewalls 352 of pillars 334A through 334D and on exposed surfaces of intrinsic poly-silicon layer 358.

Next, a brief oxide etch is used to expose the top surface of intrinsic poly-silicon layer 358. Layer 358 is then selectively etched to remove the remaining intrinsic poly-silicon using an etchant such as KOH and alcohol, ethylene and pyrocatechol or gallic acid (as described in U.S. Patent No. 5,106,987 issued to W.D. Pricer). Next, an oxide layer is deposited by, for example, chemical vapor deposition to fill the space vacated by layer 358 and to fill in between word line conductors 366. Additionally conventional process steps are used to add bit lines 368 so as to produce the structure shown in Figure 5M including memory cells 369A through 369D.

Conclusion

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. For example, the semiconductor materials and dimensions specified in this application are given by way of example and not by way of limitation. Other appropriate material can be substituted without departing from the spirit and scope of the invention.

What is claimed is:

1. A memory cell for a memory array in a folded bit line configuration, the memory cell comprising:

an access transistor formed in a pillar of single crystal semiconductor material, the access transistor having first and second source/drain regions and a body region that are vertically aligned;

the access transistor further including a gate coupled to a word line disposed adjacent to the body region;

a passing word line separated from the gate by an insulator for coupling to other memory cells adjacent to the memory cell; and

a trench capacitor, wherein the trench capacitor includes a first plate that is formed integral with the first source/drain region of the access transistor and a second plate that is disposed adjacent to the first plate and separated from the first plate by a gate oxide.

2. The memory cell of claim 1, wherein the second plate of the trench capacitor surrounds the second source/drain region.

3. The memory cell of claim 1, wherein the second plate comprises poly-silicon.

4. The memory cell of claim 1, and further comprising an ohmic contact that couples the second plate to a layer of semiconductor material.

5. A memory device, comprising:

an array of memory cells, each memory cell including a vertical access transistor formed of a single crystalline semiconductor pillar that extends outwardly from a substrate with body and first and second source/drain regions, a gate disposed adjacent

to a side of the pillar adjacent to the body region and a trench capacitor wherein a first plate of the trench capacitor is integral with the first source/drain region and a second plate of the trench capacitor is disposed adjacent to the first plate;

a number of bit lines that are each selectively coupled to a number of the memory cells at the second source/drain region of the access transistor so as to form columns of memory cells in a folded bit line configuration; and

a number of word lines disposed substantially orthogonal to the bit lines in trenches between rows of the memory cells, wherein each trench includes two word lines, each word line coupled to gates of alternate access transistors on opposite sides of the trench.

6. The memory device of claim 5, wherein the pillars extend outwardly from a semiconductor portion of the substrate.

7. The memory device of claim 5, wherein a surface area of the memory cell is $4F^2$, where F is a minimum feature size.

8. The memory device of claim 5, wherein the second plate of the trench capacitor surrounds the second source/drain region of the access transistor.

9. The memory device of claim 5, wherein the second plate of the trench capacitor is maintained at approximately ground potential.

10. The memory device of claim 5, wherein the second plate of the trench capacitor comprises poly-silicon that is maintained at a constant potential.

11. The memory device of claim 5, wherein the pillar has a sub-micron width so as to allow substantially full depletion of the body region.

12. The memory device of claim 5, wherein the word lines are sub-lithographic.

13. A memory array comprising:

a number of memory cells forming an array with a number of rows and columns, each memory cell including an access transistor having body and first and second source/drain regions formed vertically, outwardly from a substrate and a gate disposed adjacent to a side of the transistor, the second source/drain region including an upper semiconductor surface;

a number of first isolation trenches separating adjacent rows of memory cells;

first and second word lines disposed in each of the first isolation trenches and coupled to alternate gates on opposite sides of the trench; and

a number of second isolation trenches, each substantially orthogonal to the first isolation trenches and interposed between adjacent memory cells.

14. The memory array of claim 13, wherein the gates of the access transistors are each formed integral with one of the word lines.

15. The memory array of claim 13, wherein the pillars extend outwardly from a semiconductor portion of the substrate.

16. The memory array of claim 13, wherein a surface area of the memory cell is $4F^2$, where F is a minimum feature size.

17. The memory array of claim 13, wherein the second plate of the trench capacitor surrounds the second source/drain region of the access transistor.

18. The memory array of claim 13, wherein the second plate of the trench capacitor comprises poly-silicon that is maintained at a constant potential.

19. The memory array of claim 13, wherein the word lines have a width that is less than the minimum feature size, F.

20. A method of fabricating a memory array, the method comprising the steps of :

forming a number of access transistors, each access transistor formed in a pillar of semiconductor material that extends outwardly from a substrate wherein the access transistor includes a first source/drain region, a body region and a second source/drain region formed vertically thereupon;

forming a trench capacitor, wherein a first plate of the trench capacitor is integral with the first source/drain region of the access transistor;

forming a number of word lines in a number of trenches that separate adjacent rows of access transistors, wherein each trench includes two word lines with a gate of each word line interconnecting alternate access transistors on opposite sides of the trench; and

forming a number of bit lines that interconnect second source/drain regions of selected access transistors.

21. The method of claim 20, wherein the step of forming a trench capacitor further includes the step of forming a second plate that surrounds the first plate.

22. The method of claim 20, and further comprising the step of forming a contact that couples a second plate of the trench capacitor to an underlying semiconductor layer.

23. The method of claim 20, where the step of forming a trench capacitor comprises the step of forming a second plate that forms a grid pattern in a layer of semiconductor material such that the grid surrounds each of the pillars that form the access transistors.

24. The method of claim 20, wherein the step of forming a trench capacitor comprises the step of depositing poly-silicon in crossing row and column isolation trenches formed around the pillars that define the access transistors.

25. A method of fabricating a memory array, the method comprising the steps of:

forming a first conductivity type first source/drain region layer on a substrate;

forming a second conductivity type body region layer on the first source/drain region layer;

forming a first conductivity type second source/drain region layer on the body region layer;

forming a plurality of substantially parallel column isolation trenches extending through the second source/drain region layer, the body region layer, and the first source/drain region layer, thereby forming column bars between the column isolation trenches;

forming a plurality of substantially parallel row isolation trenches, orthogonal to the column isolation trenches, extending to substantially the same depth as the column isolation trenches, thereby forming an array of vertical access transistors for the memory array;

filling the row and column isolation trenches with a conductive material to a level that does not exceed the lower level of the body region so as to provide a common plate for capacitors of memory cells of the memory array;

forming two conductive word lines in each row isolation trenches that selectively interconnect alternate access transistors on opposite sides of the row isolation trench; and

forming bit lines that selectively interconnect the second source/drain regions of the access transistors on each column.

26. The method of claim 25, wherein the step of forming a first conductivity type first source/drain region layer on a substrate comprises the step of forming first

conductivity type first source/drain region layer on a substrate that extends outwardly from the substrate to a distance sufficient for the source/drain region layer to also function as a first plate of the capacitor for each memory cell in the array.

Abstract of the Disclosure

A memory cell for a memory array in a folded bit line configuration. The memory cell includes an access transistor formed in a pillar of single crystal semiconductor material. The access transistor has first and second source/drain regions and a body region that are vertically aligned. The access transistor further includes a gate coupled to a wordline disposed adjacent to the body region. The memory cell also includes a passing wordline that is separated from the gate by an insulator for coupling to other memory cells adjacent to the memory cell. The memory cell also includes a trench capacitor. The trench capacitor includes a first plate that is formed integral with the first source/drain region of the access transistor. The trench capacitor also includes a second plate that is disposed adjacent to the first plate and separated from the first plate by a gate oxide.

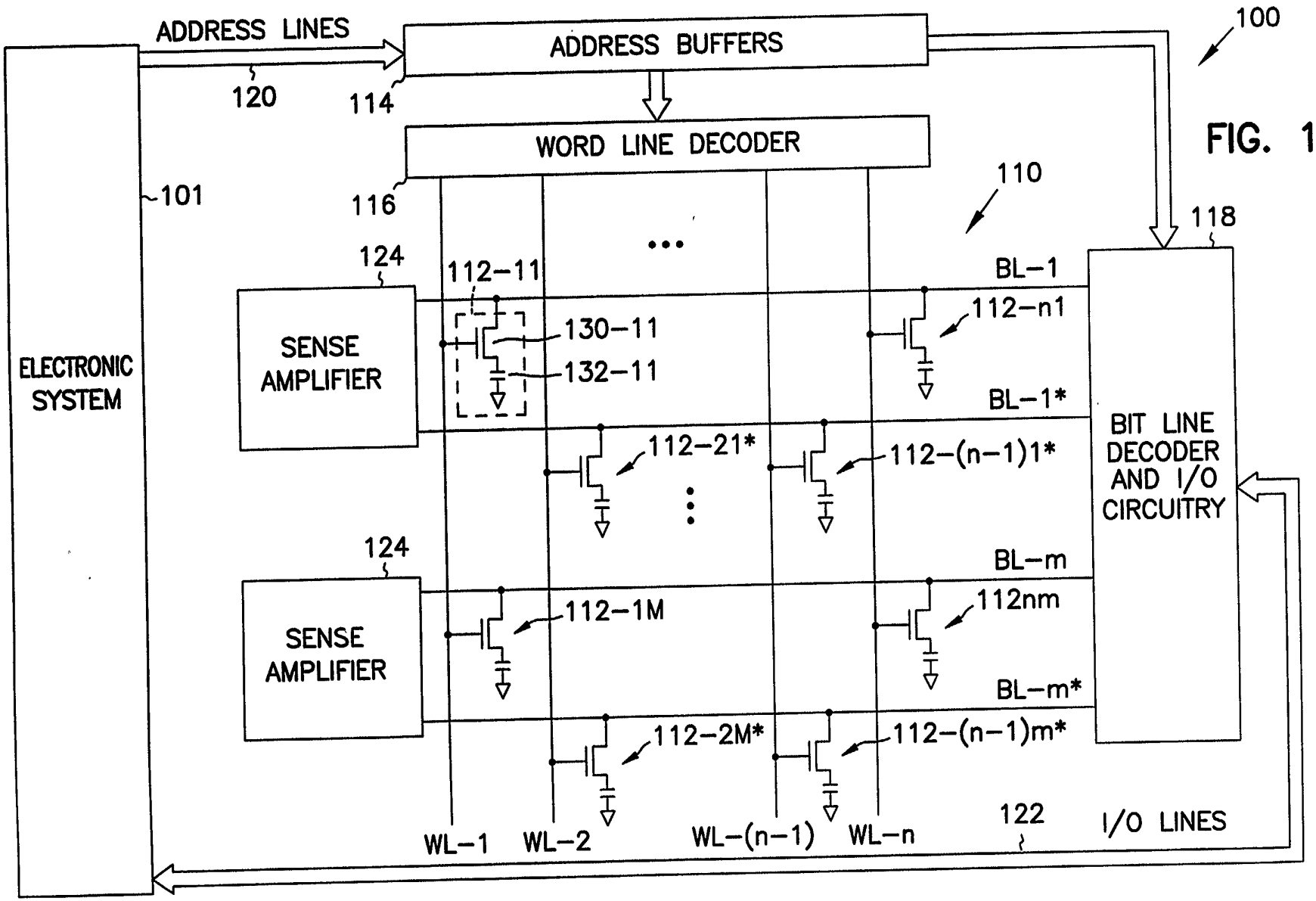

FIG. 1

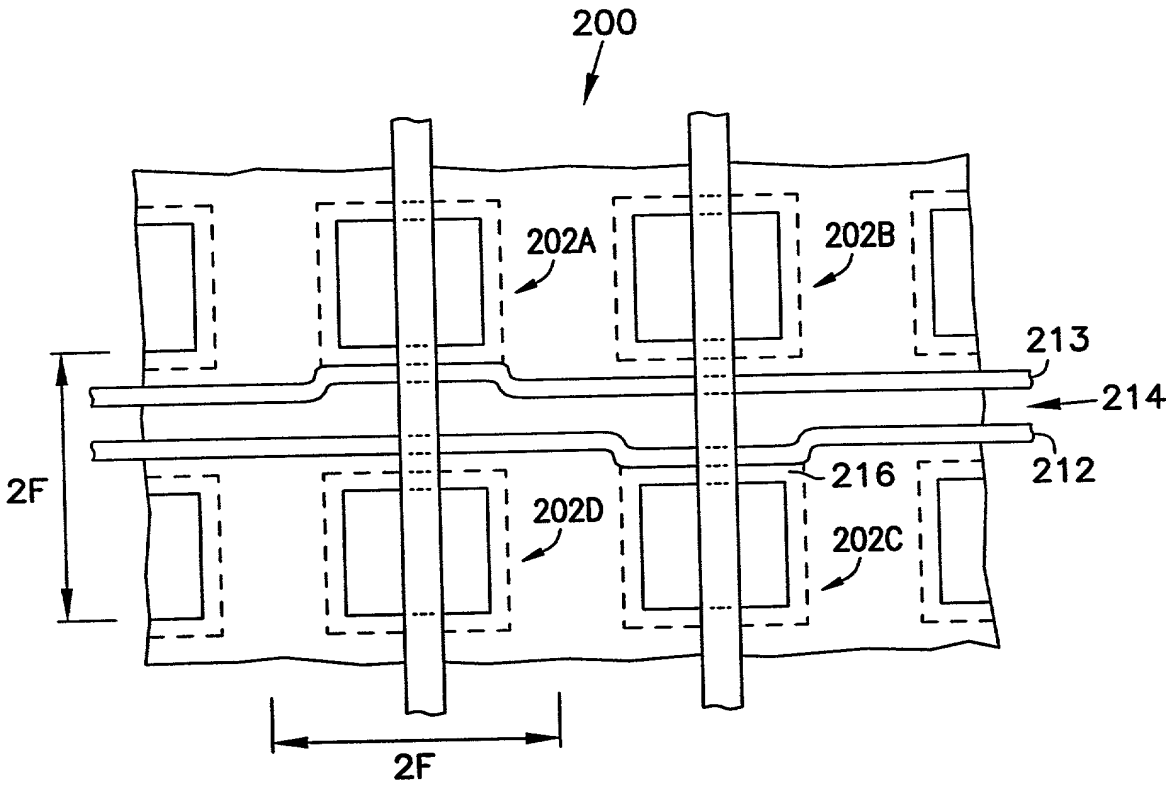

FIG. 2

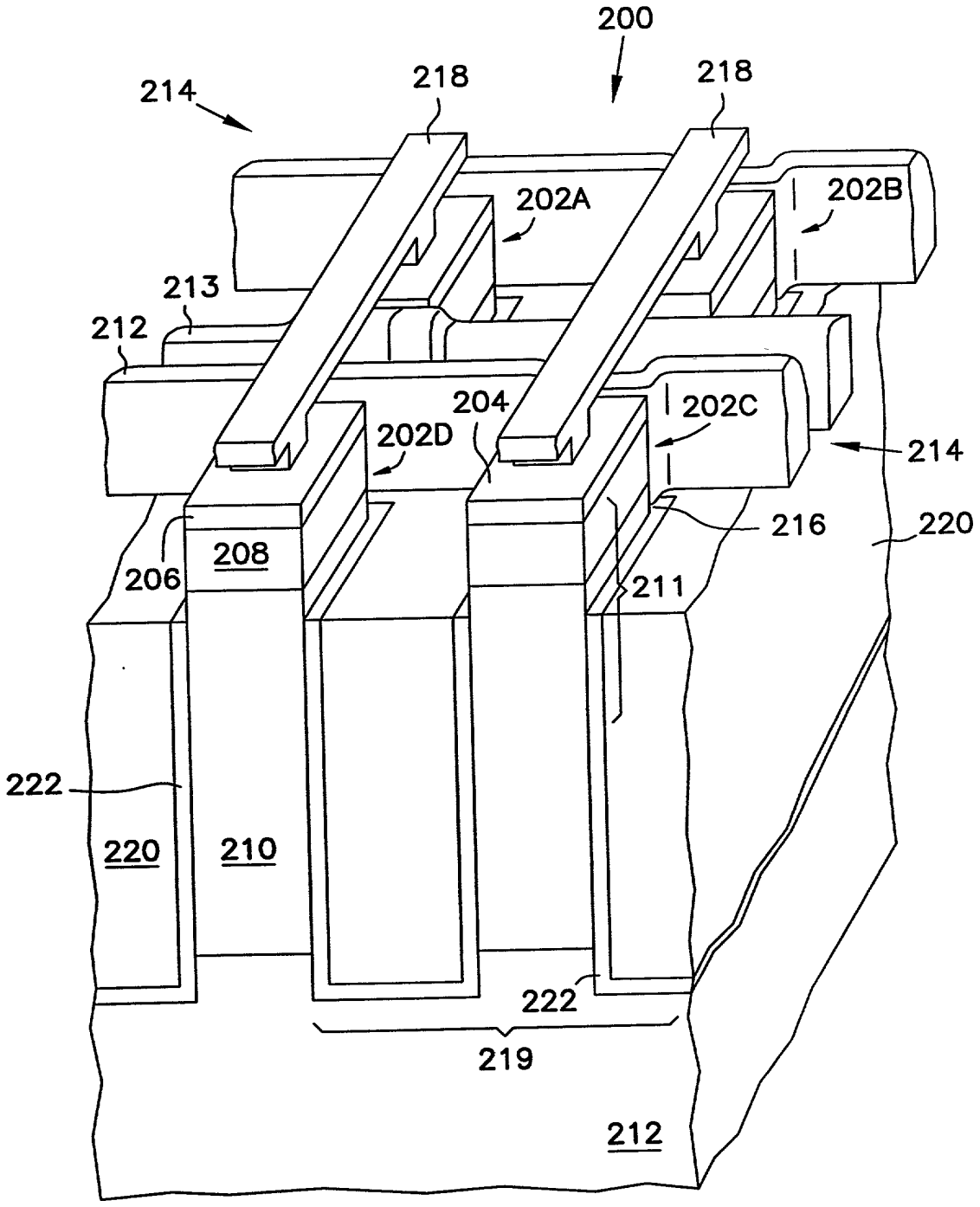
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FIG. 3

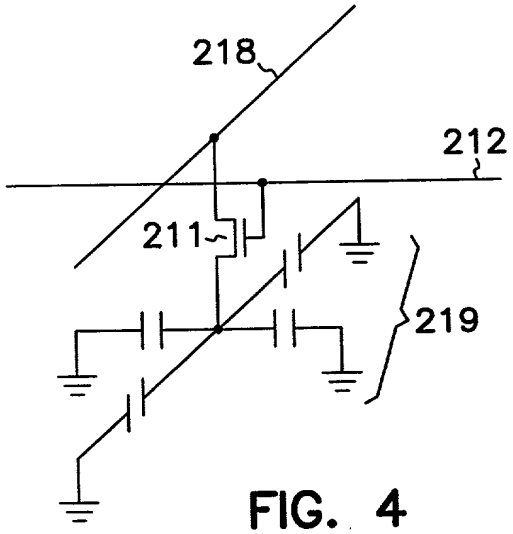

FIG. 4

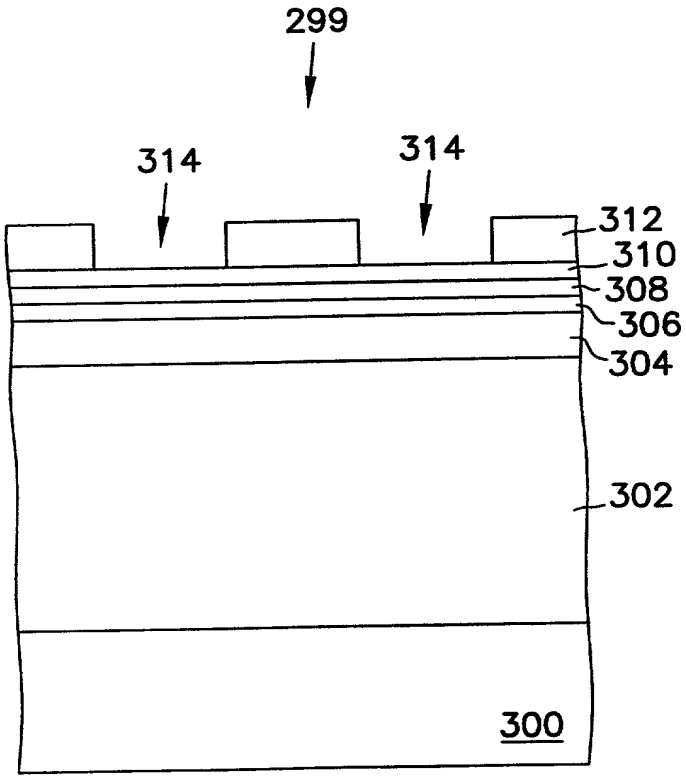

FIG. 5A

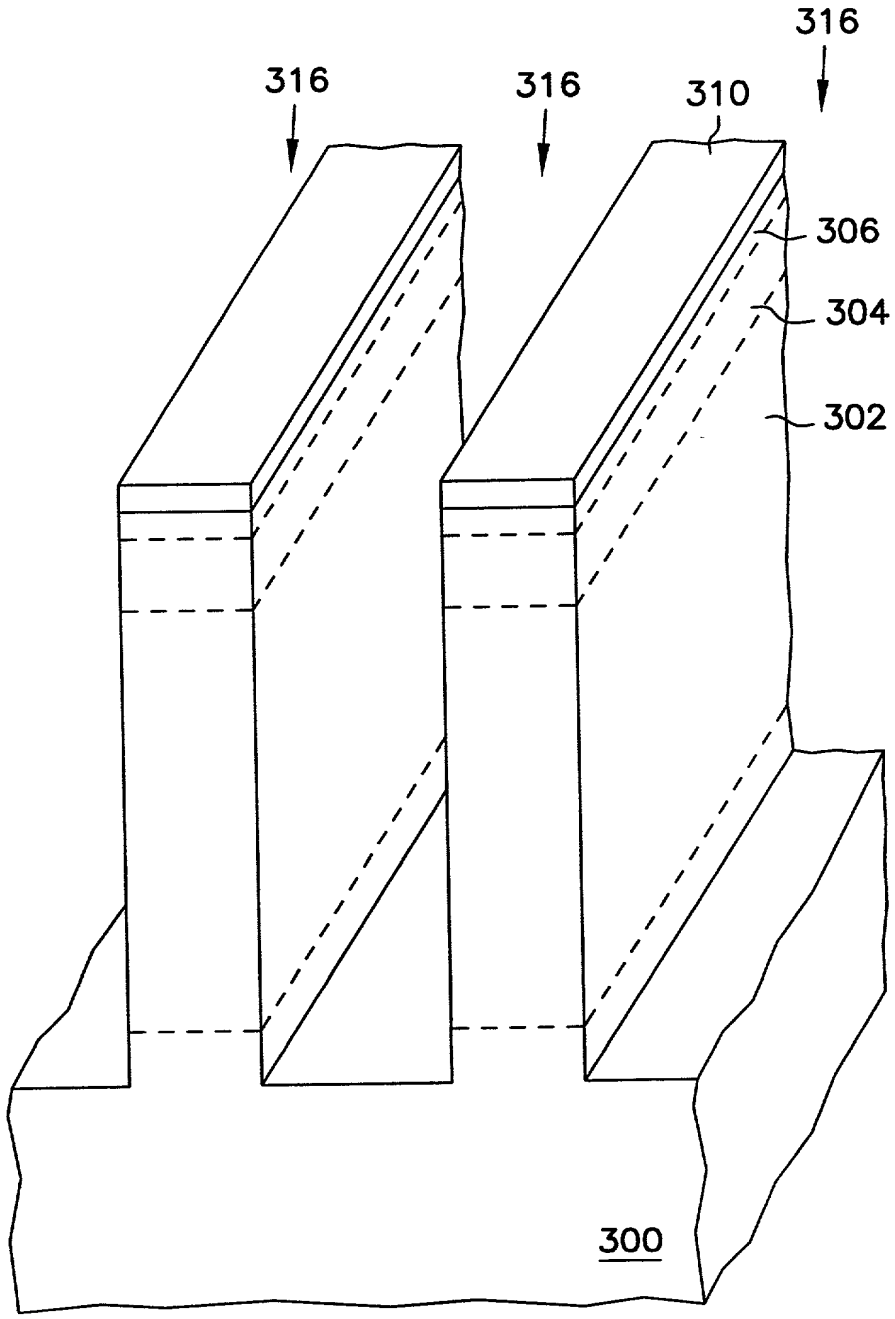

FIG. 5B

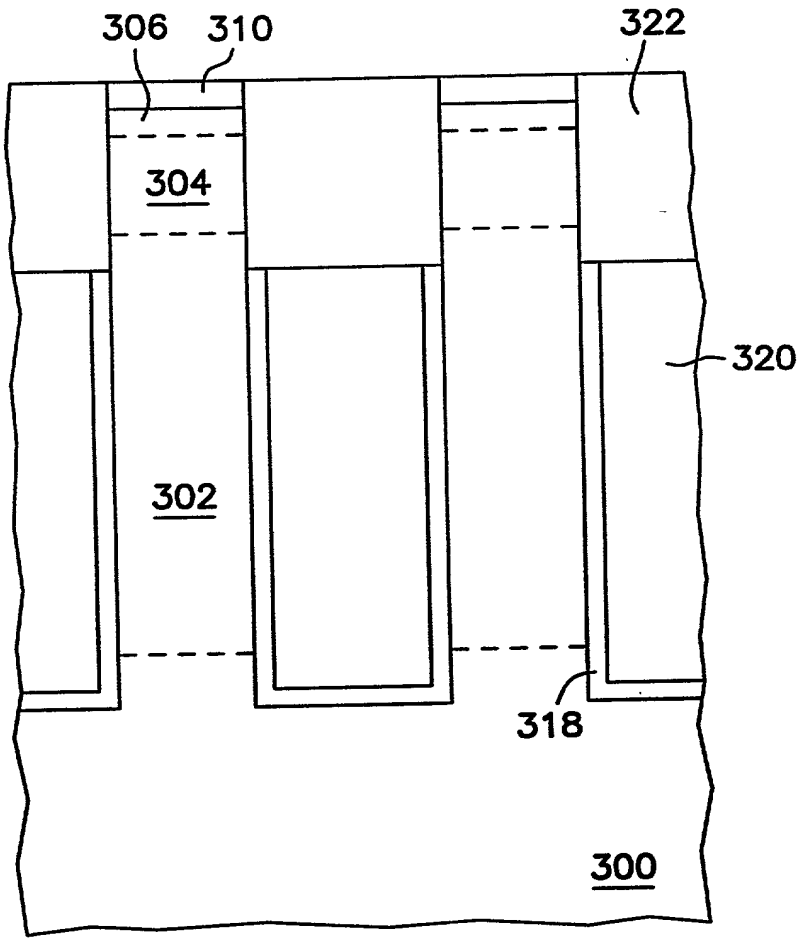

FIG. 5C

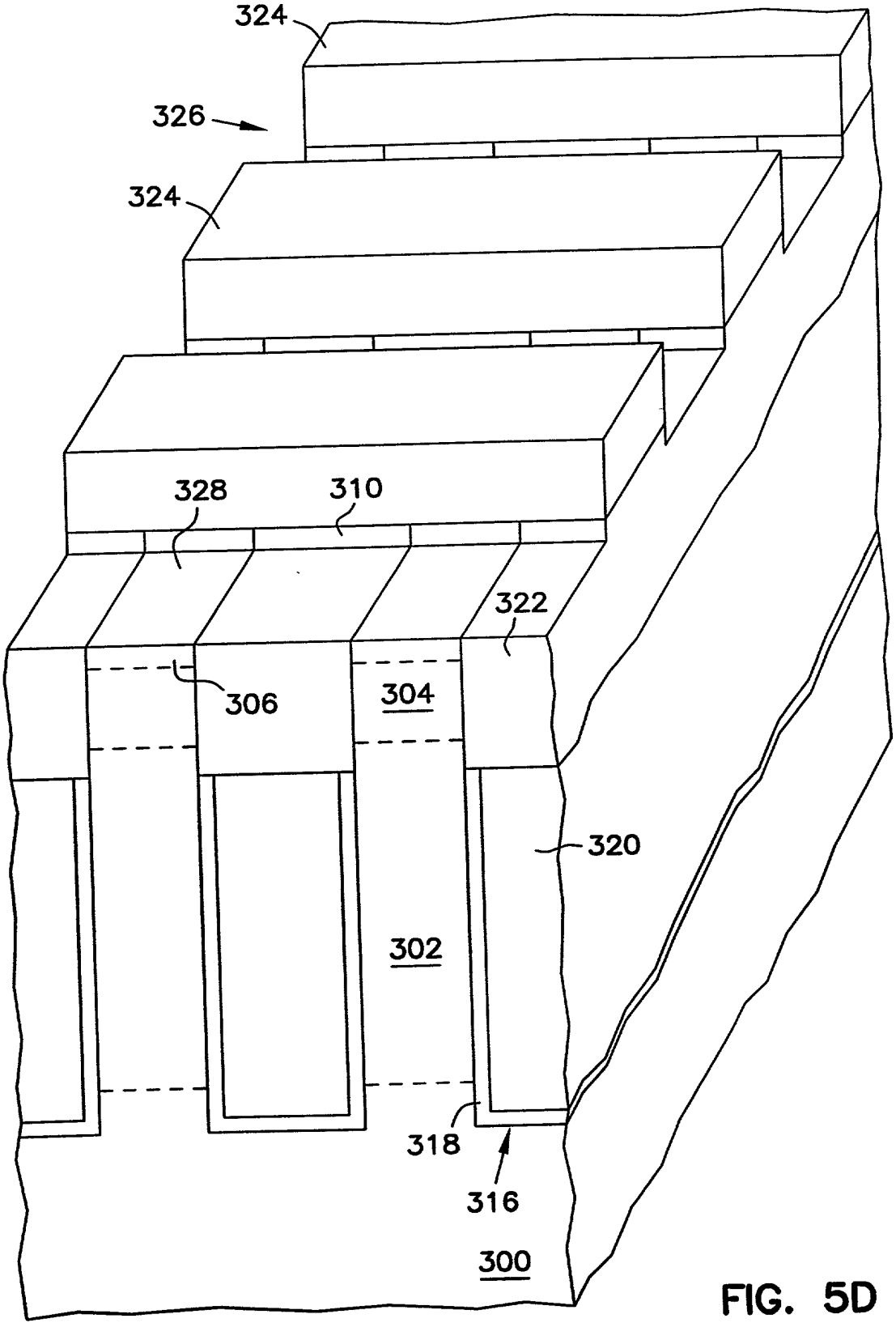

FIG. 5D

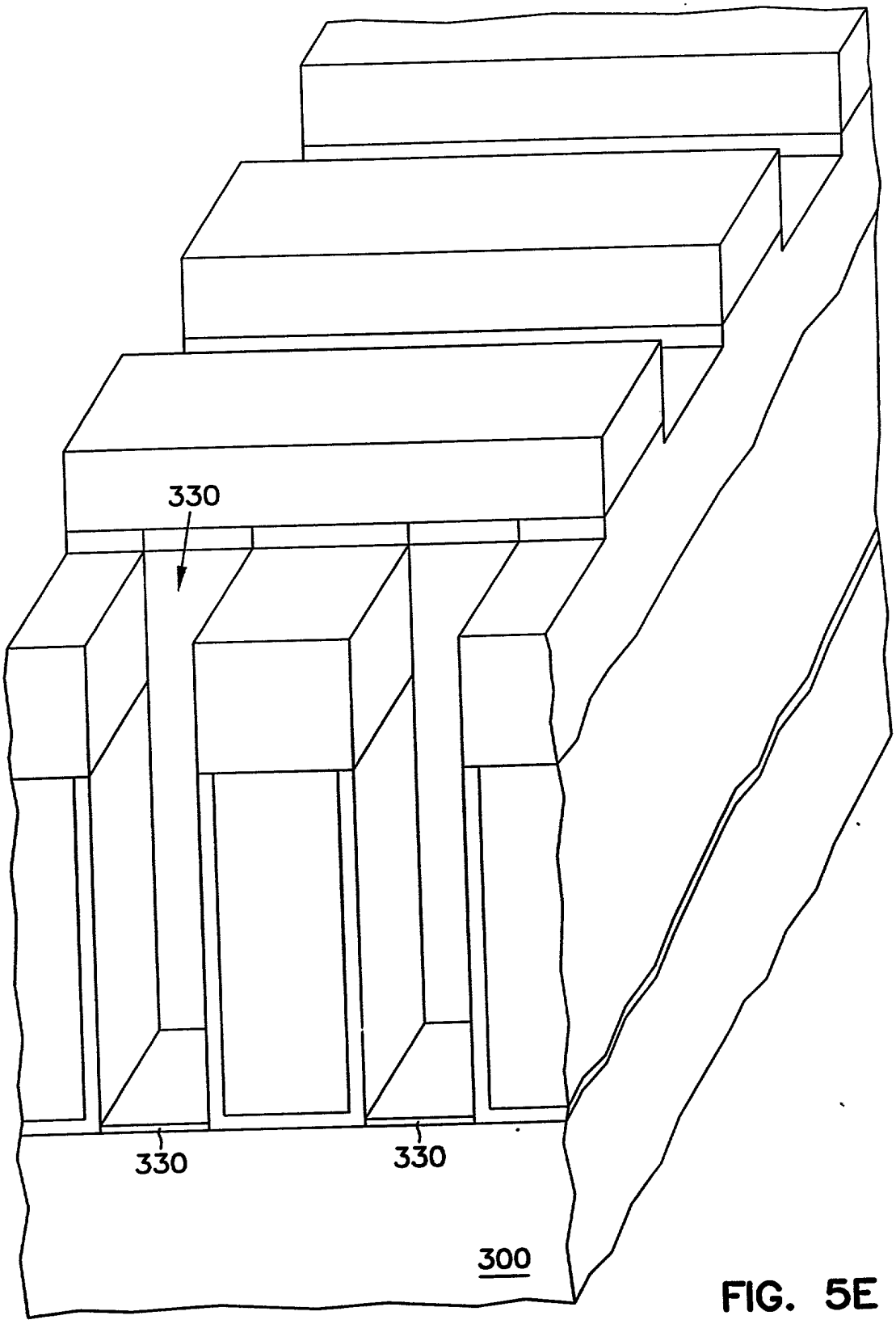

FIG. 5E

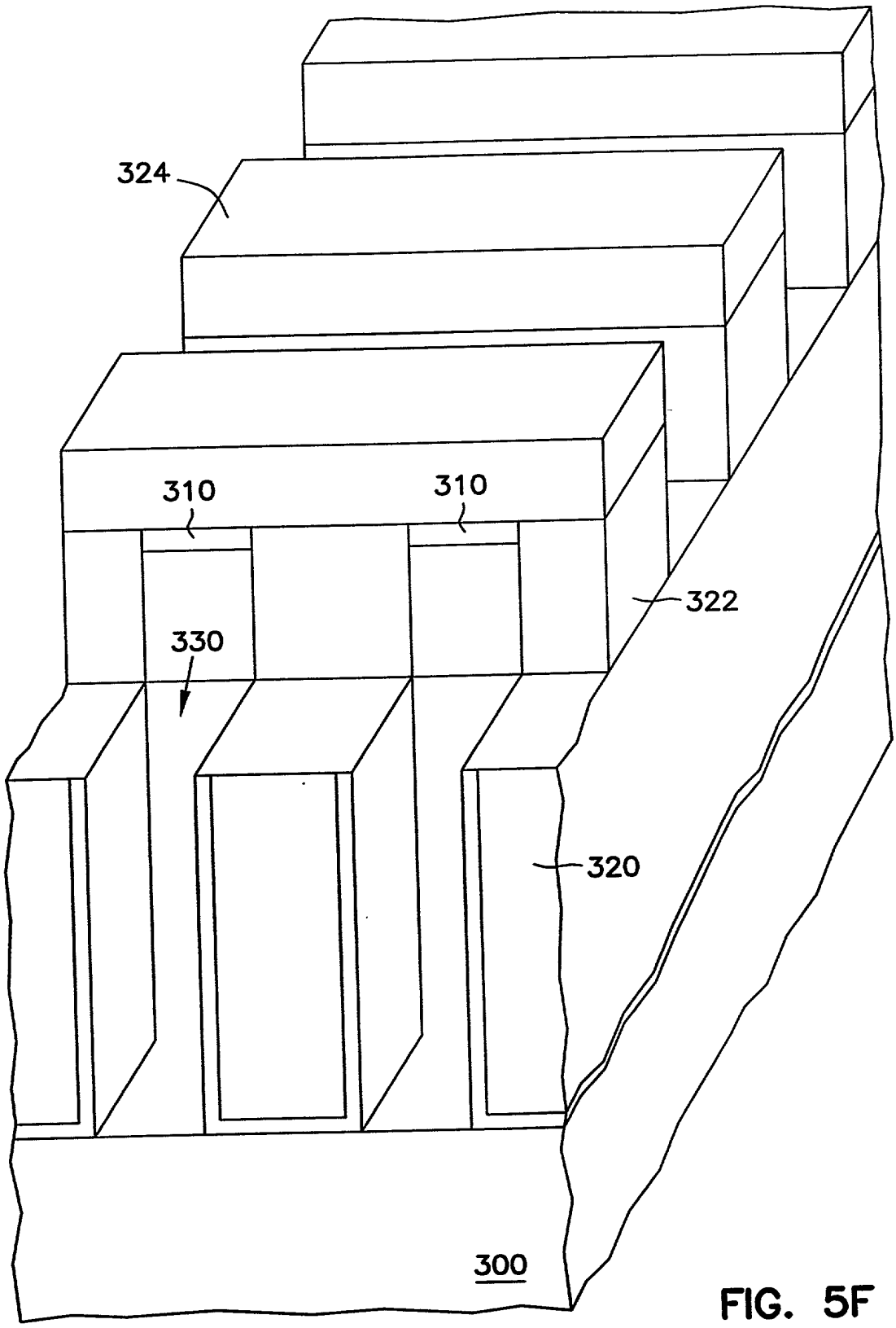

FIG. 5F

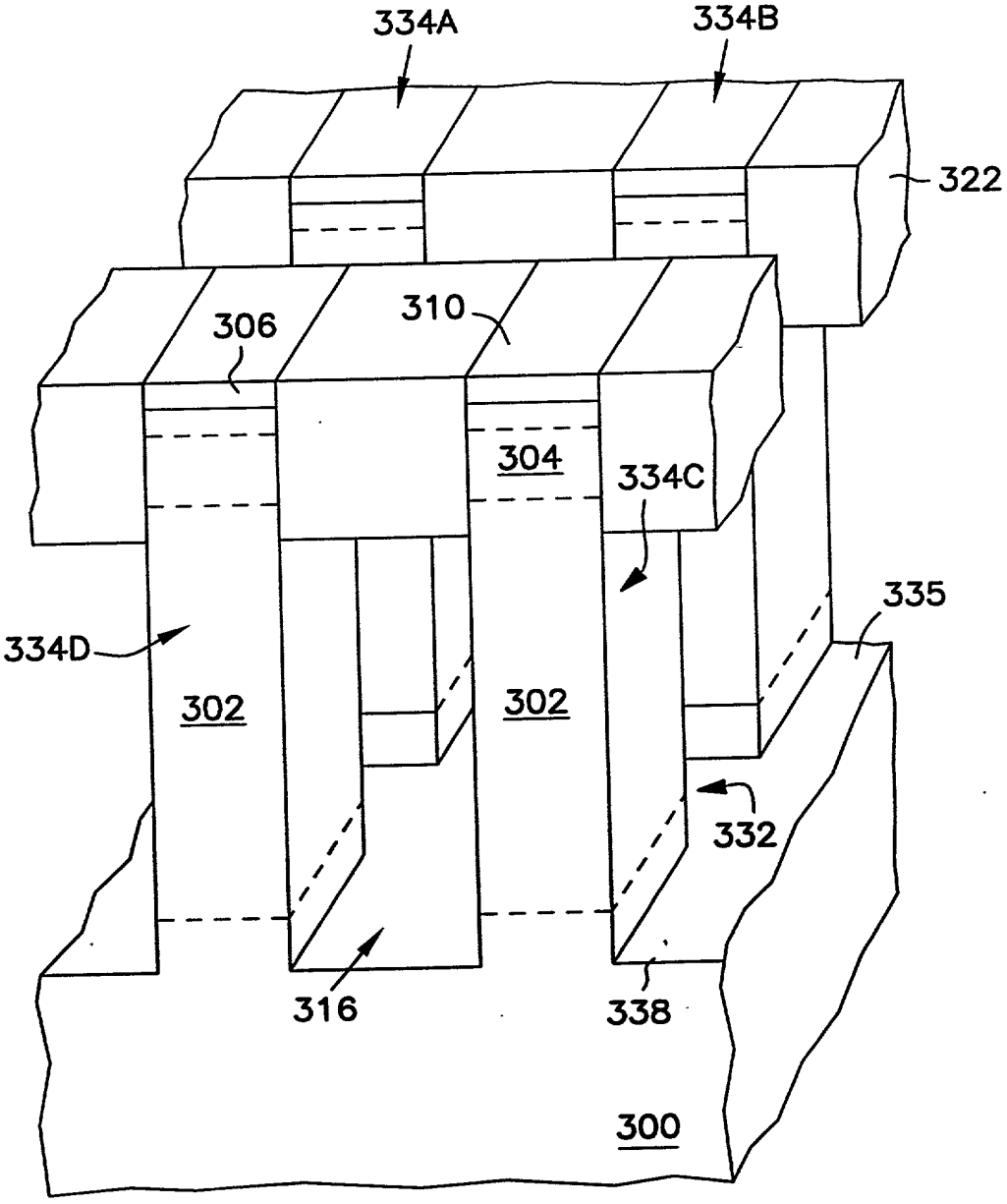

FIG. 5G

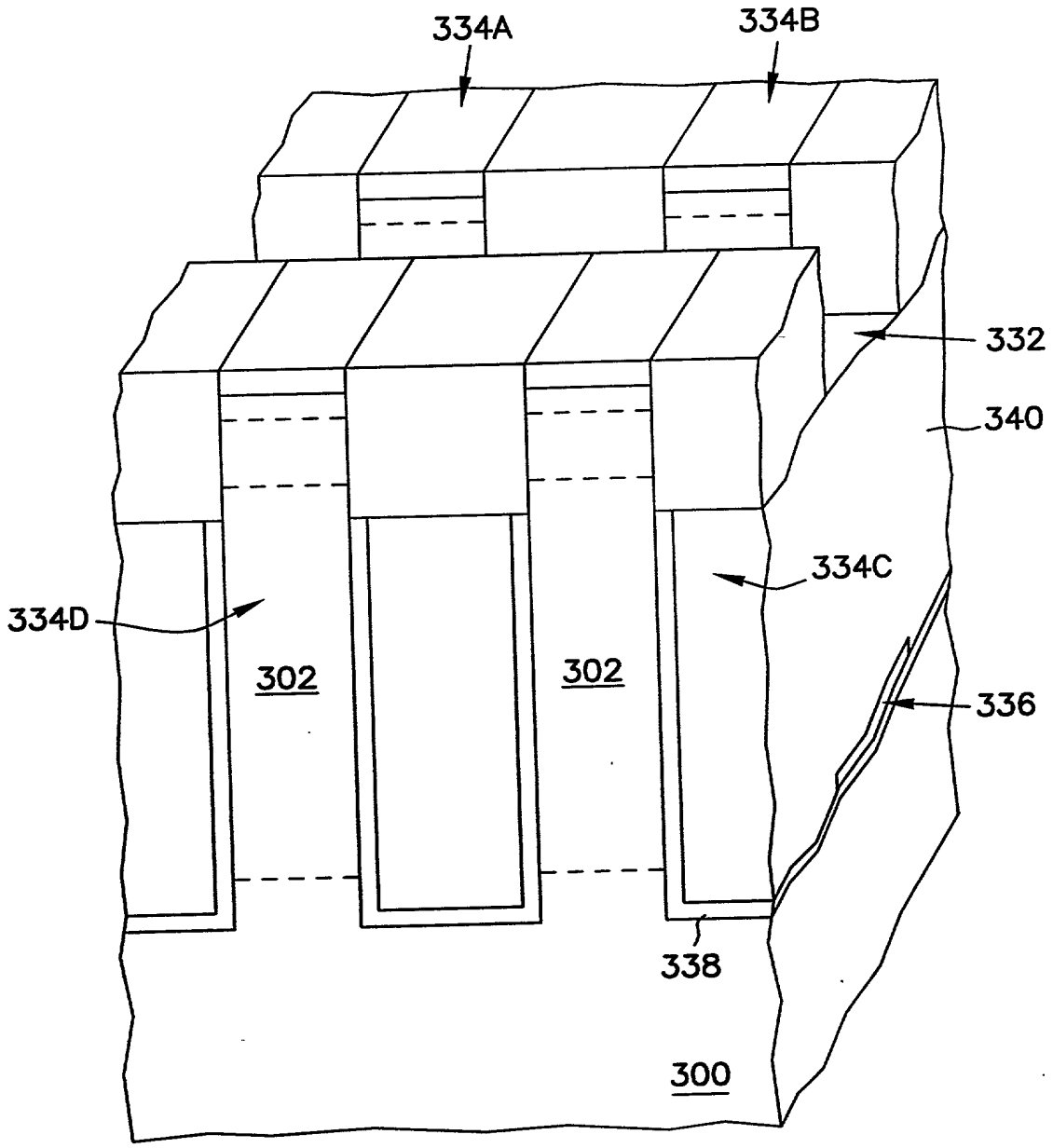

FIG. 5H

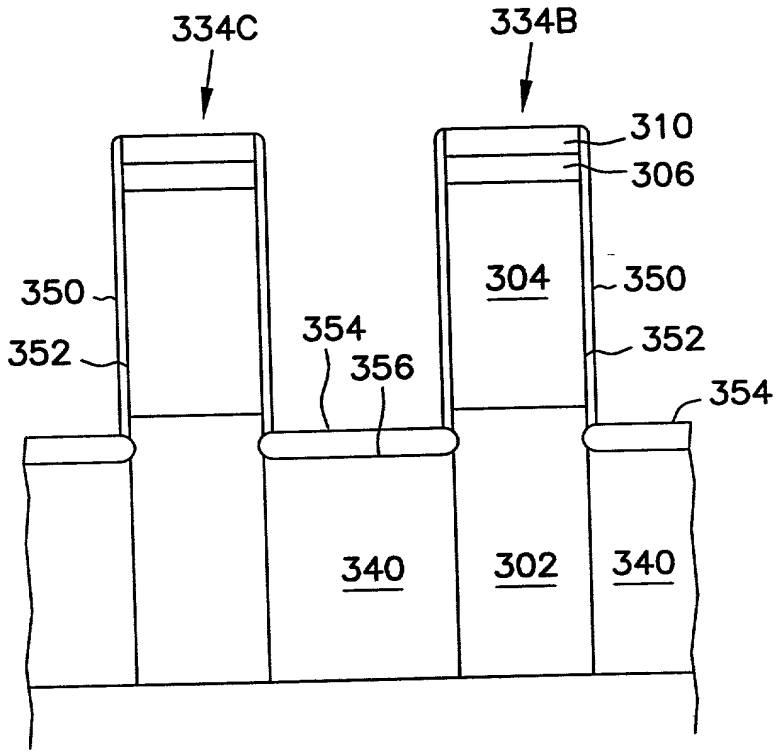

FIG. 5I

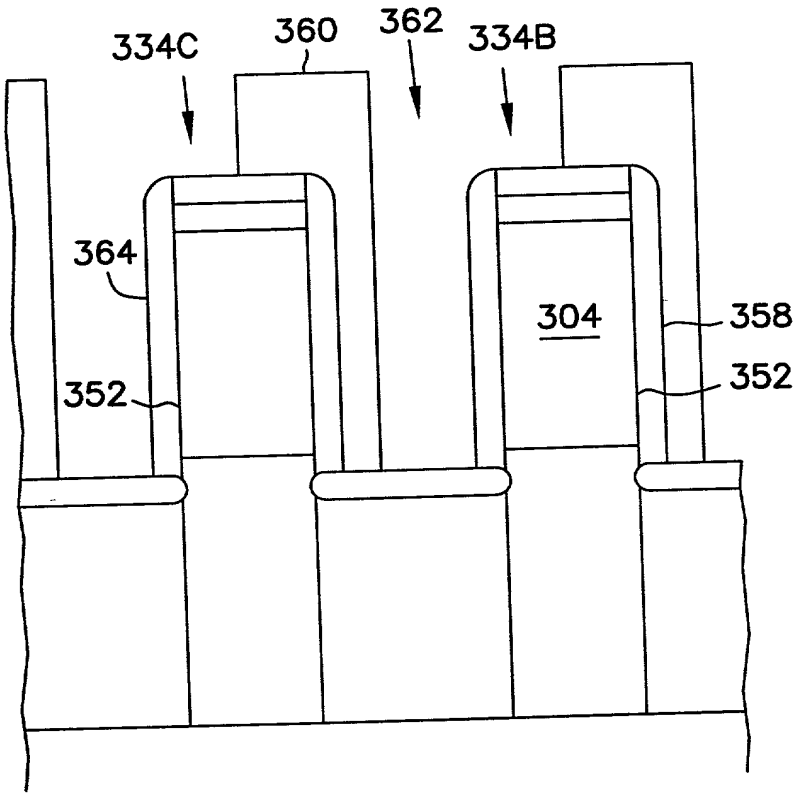

FIG. 5J

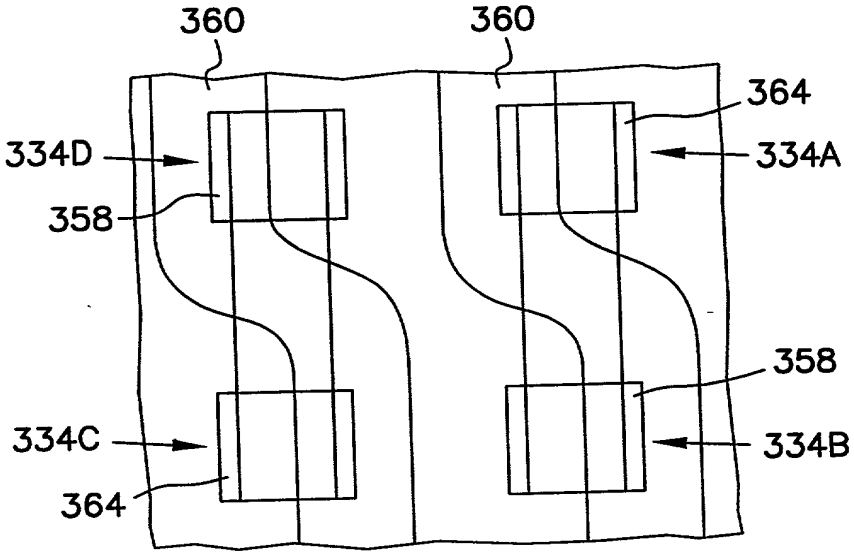

FIG. 5K

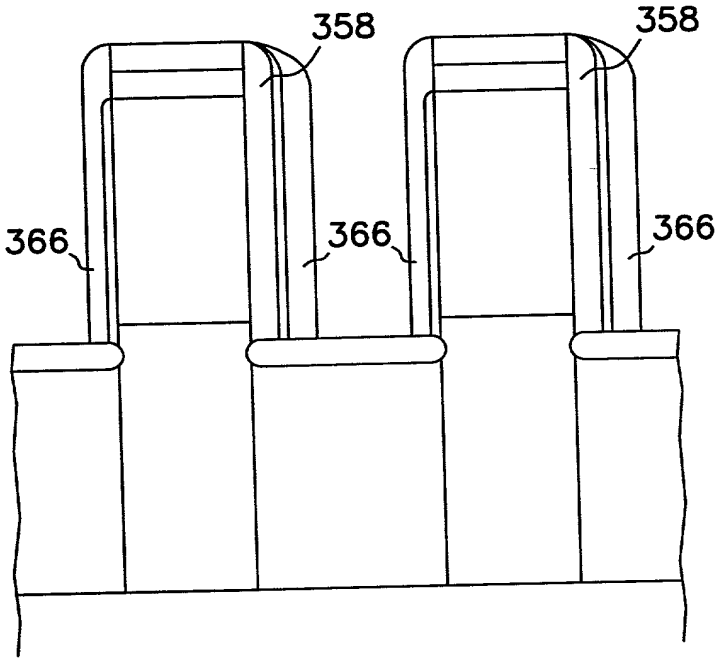

FIG. 5L

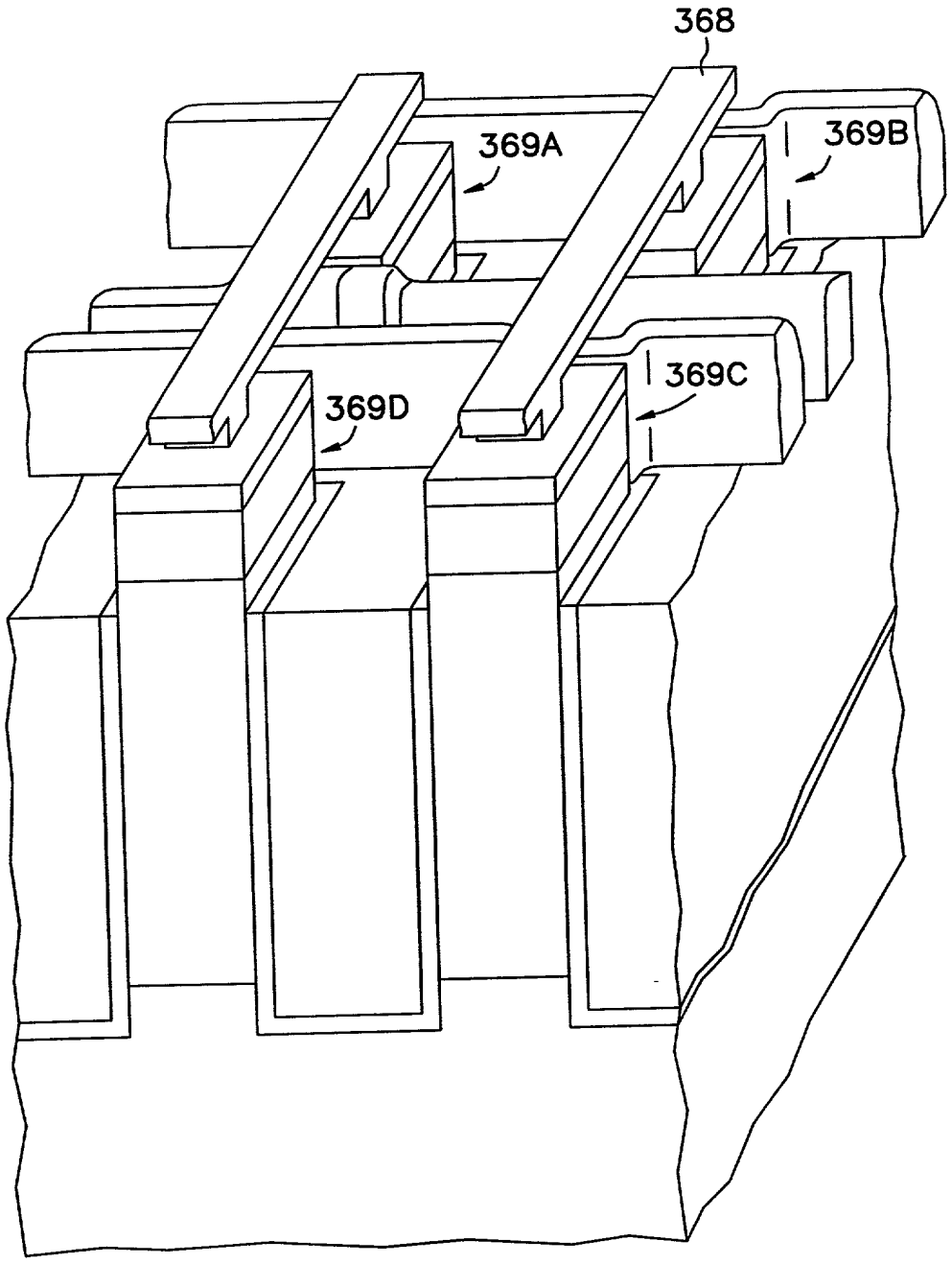

FIG. 5M

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR.

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such applications have been filed.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

No such applications have been filed.

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

No such applications have been filed.

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

Bianchi, Timothy E.	Reg. No. 39,610	Fogg, David N.	Reg. No. 35,138	Lundberg, Steven W.	Reg. No. 30,568
Billig, Patrick G.	Reg. No. 38,080	Forrest, Bradley A.	Reg. No. 30,837	Lynch, Michael L.	Reg. No. 30,871
Billion, Richard E.	Reg. No. 32,836	Harris, Robert J.	Reg. No. 37,346	Madrid, Andres N.	Reg. No. 40,710
Brennan, Thomas F.	Reg. No. 35,075	Hofmann, Rudolph P., Jr.	Reg. No. 38,187	Pappas, Lia M.	Reg. No. 34,095
Brooks, Edward J., III	Reg. No. 40,925	Holloway, Sheryl S.	Reg. No. 37,850	Schwegman, Micheal L.	Reg. No. 25,816
Clark, Barbara J.	Reg. No. 38,107	Klima-Silberg, Catherine I.	Reg. No. 40,052	Simboli, Paul B.	Reg. No. 38,616
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Dryja, Michael A.	Reg. No. 39,662	Lemaire, Charles A.	Reg. No. 36,198	Viksnins, Ann S.	Reg. No. 37,748
Embretson, Janet E.	Reg. No. 39,665	Litman, Mark A.	Reg. No. 26,390	Woessner, Warren D.	Reg. No. 30,440
Farney, W. Bryan	Reg. No. 32,651				

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/organization/who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Schwegman, Lundberg, Woessner & Kluth, P.A. to the contrary.

Please direct all correspondence in this case to Schwegman, Lundberg, Woessner & Kluth, P.A. at the address indicated below:

P.O. Box 2938, Minneapolis, MN 55402

Telephone No. (612)373-6900

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of joint inventor number 1 : **Wendell P. Noble**
Citizenship: **United States of America** Residence: **Milton, VT**
Post Office Address: 84 Swamp Road
Milton, VT 05468

Signature: Wendell P. Noble Date: 9/16/97
Wendell P. Noble

Full Name of joint inventor number 2 : **Leonard Forbes**
Citizenship: **United States of America** Residence: **Corvallis, OR**
Post Office Address: 965 NW Highland Terrace
Corvallis, OR 97330

Signature: _____ Date: _____
Leonard Forbes

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR.**

The specification of which is attached hereto.

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P.O. Box 2938, Minneapolis, MN 55402

Telephone No. (612)373-6900

Our Ref. 303.379US1
Serial No. not assigned
Filing Date: not assigned

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Post Office Address: 84 Swamp Road
Milton, VT 05468

Signature: _____ Date: _____
Wendell P. Noble

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Citizenship: **United States of America** Residence: **Corvallis, OR**
Post Office Address: 965 NW Highland Terrace
Corvallis, OR 97330

Signature: _____ Date: 18 SEPT 97
Leonard Forbes

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

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(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.